REMARKS

In response to the Office Action mailed July 24, 2006, Applicants respectfully request reconsideration. Claims 1-32 were previously pending in this application. Claims 1, 9, 13, 20, 21 and 26 have been amended for clarity. As a result, claims 1-32 are pending for examination with claims 1 and 13 being independent claims. No new matter has been added.

Objections to the Drawings

The Office Action objected to the drawings because the feature recited in claim 10 is purportedly not shown in the drawings. Applicants respectfully disagree. The limitation of claim 10 is illustrated in FIG. 3, which illustrates one embodiment in which a regulator circuit includes differential amplifiers 126 and 130. In this embodiment, the drain terminal 14a is maintained at a voltage equal to the reference voltage V_{REF}. Accordingly, withdrawal of this objection is respectfully requested.

Objections to the Claims

The Office Action objected to claims 20, 23, 26 and 27. The Office Action indicated that the limitation "a comparator" is purportedly claimed twice in claims 20 and 26, and that the limitation "a first feedback amplifier" is purportedly claimed twice in claims 23 and 27. Applicants respectfully point out that the recitation of these limitations is appropriate. Claim 26 does not depend from claim 20, and claims 20 and 26 have different scope. Applicants further point out that claim 23 does not depend from claim 27, and claims 23 and 27 have different scope. The limitations "a comparator" and "a first feedback amplifier" are appropriately recited in these claims. Accordingly, withdrawal of this objection is respectfully requested.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-9 and 11-32 under 35 U.S.C. §103(a) as being unpatentable over Pollachek, U.S. Patent No. 4,648,074, in view of Lee et al., U.S. Patent No. 5,909,405, Garni et al., U.S. Patent No. 6,621,729 and Passotti et al., U.S. Patent No. 6,535,428. Applicants respectfully request reconsideration.

The Office Action relies primarily on the Pollachek reference in rejecting claims of the present application. As discussed in a previous response, Pollachek is directed to a reference

circuit with a semiconductor memory array (Title). FIG. 3 illustrates a memory stack that forms a data storage portion of memory array 30 (col. 3, lines 43-45). A bit line of the memory stack is connected to one input of differential amplifier 22, which is used for reading the contents of the memory stack (col. 3, lines 55-56). Before the memory stack is read, the bit line is precharged to V_{DD} volts by applying a "precharge pulse (PC) to the gate electrode of PT1 which turns PT1 on momentarily" (col. 3, lines 61-64). Thus, transistor PT1 is not a load transistor, but merely a switching transistor that momentarily turns on prior to read-out to charge the bit line to the voltage V_{DD} so that the contents of the memory stack can be read (col. 5, lines 52-64). Transistors PT1 and PT2 are off during the reading of the memory cells, so that memory cells can be read out.

By contrast, claim 1 as amended recites, *inter alia*, that the first load is controlled to provide a reading current to the reference cell during a reading of the non-volatile memory cell. Pollachek does not teach or suggest a first load that is controlled to provide a reading current to a reference cell during a reading of a non-volatile memory cell. Rather, transistors PT1 and PT2, relied upon in the Office Action, are turned off during the reading of a memory cell in Pollachek's implementation. Lee et al., Garni et al. and Pasotti et al. fail to remedy this deficiency. Therefore, claim 1 patentably distinguishes over the combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 2-12 depend from claim 1 and are therefore patentable for at least the same reasons.

Claim 13, as amended, recites, *inter alia*, that the first transistor is controlled to provide a reading current to the reference memory cell during a reading of the memory cell. Pollachek does not teach or suggest a first transistor controlled to provide a reading current to a reference memory cell during a reading of the memory cell. Again, transistors PT1 and PT2 of Pollachek are turned off during the reading process. Lee et al., Garni et al. and Pasotti et al. fail to remedy this deficiency. Therefore, claim 13 patentably distinguishes over the combination. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 14-32 depend from claim 13 and are therefore patentable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: November 21, 2006

Respectfully submitted,

By: _____

James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Tel.: (617) 646-8000